**What Is Claimed Is**:

1. A method of driving a liquid crystal display, comprising:

dividing input data into most significant bit data and least significant bit data;

delaying the most significant bit data for one frame period; and

modulating the most significant bit data in accordance with a difference between the delayed most significant bit data and the current most significant bit data, wherein the modulated data have a data width not wider than that of the input data and not narrower than that of the most significant bit data.

2. The method according to claim 1, wherein each most significant bit data and each least significant bit data are 4 bits, and each input data and the modulated data are 8 bits.

3. The method according to claim 1, further comprising:

attaching the least significant bit data of a current frame to the modulated data.

4. The method according to claim 1, wherein the modulating the most significant bit data comprises,

comparing the current most significant bit data with the one frame period delayed most significant bit data;

selecting desirable data from a look-up table based on the compared data; and

outputting the selected data corresponding to the current most significant bit data.

5. A driving apparatus for a liquid crystal display, comprising:

a memory receiving most significant bits of an $n^{th}$ frame from an input line and outputting the most significant bits of an $(n-1)^{th}$ frame; and

a modulator modulating the most significant bits of an $n^{th}$ frame in accordance to a difference between the most significant bits of the $(n-1)^{th}$ frame and the $n^{th}$ frame, wherein the modulated

most significant bits have a data width not wider than that of the input data and not narrower than that of the most significant bits of the $(n-1)^{th}$ frame (wherein n is positive integer).

6. The apparatus according to claim 5, wherein each most significant bit and each least significant bit have 4 bits, and each input data and each modulated data have 8 bits.

7. The apparatus according to claim 5, wherein the modulator includes a look-up table having the modulated data.

8. The apparatus according to claim 5, further comprising:

a liquid crystal display panel having a plurality of data lines to which data are supplied and a plurality of gate lines to which scanning signals are supplied;

a data driver receiving modulated video data from the data modulator, adding the least significant bits bypassed from the input line, and supplying the modulated video data to the data lines;

a gate driver supplying the scanning signals to the gate

lines; and

a timing controller supplying the video data to the input line and concurrently controlling the data driver and the gate driver.

9. A liquid crystal display comprising:

a liquid crystal display panel displaying images and having a plurality of data lines and a plurality of gate lines thereon;

a timing controller rearranging video data received from an input data and outputting RGB data and first and second timing signals;

a data modulator modulating most significant bits of the video data based on a look-up table having a data width not wider than that of the input data and not narrower than that of the most significant bits;

a data driver receiving the modulated video data and the first timing signal, attaching least significant bits thereto, and supplying the modulated video data to the liquid crystal display panel through the data lines; and

a gate driver receiving the second timing signal and supplying a scanning signal to the liquid crystal display panel through the gate lines.

10. The liquid crystal display according to claim 9, wherein the data modulator includes a frame memory delaying current most significant bits for one frame period and outputting the delayed most significant bits and a look-up table receiving both the current most significant bits and the delayed most significant bits and outputting the modulated video data to the liquid crystal display panel.

11. The liquid crystal display according to claim 9, wherein each most significant bits and each least significant bits have 4 bits.

12. The liquid crystal display according to claim 9, wherein each input data and each modulated data have 8 bits.